Remarks/Arguments

Claims 1-33 remain in this application.

The examiner has rejected claims 1-5, 7-13, 15-26 and 28-33 under 35 U.S.C. 102(e) as being anticipated by US Patent 6,834,360 B2 to *Corti, et al.*

The examiner has rejected claims 6, 14 and 27 under 35 U.S.C. 103(a) as being unpatentable over *Corti, et al.*, in view of US Patent 6,694,489 B1 to *Case, et al.*

In view of the above amendments and these remarks, reconsideration of the above noted objections is respectfully requested.

Rejections Under 35 USC 102(e):

Applicant respectfully traverses the rejection of **claims 1-5, 7-13, 15-26 and 28-33** under 35 U.S.C. 102(e) as being anticipated by *Corti, et al.* The independent claims are **1, 11, 19, 22, 24, 29, 30 and 33** and have been amended above.

Amended independent **claim 1** recites (among other limitations):

> initiating a process in the computer system, the process including instructions and **running on a general-purpose processor** in the computer system;
>
> launching a debugger program that is embedded in a ROM of the computer system, the debugger program **running on the general-purpose processor**;
>
> executing at least part of the instructions **by the general-purpose processor**; and
>
> **interrupting execution of the instructions** in order for the debugger program to operate on at least part of the executed instructions.

Additionally, amended independent **claim 11** recites (among other limitations):

> at least one **general-purpose processor**;
>
> ...
>
> a target process having instructions, **executable by the general-purpose processor**; and
>
> a debugger program embedded within the ROM, **executable by the general-purpose processor**, to **interrupt**

execution of the instructions in order to operate on at least part of the **instructions** of the target process.

In addition, amended independent **claim 19** recites (among other limitations):

> **a general-purpose processor** in the target computer;
> a target process having instructions **executable by the general-purpose processor** in the target computer; and
> a debugger program embedded in the ROM and **executable by the general-purpose processor** in the target computer to **interrupt execution of the instructions** in order to generate data on the execution of at least part of the instructions of the target process ....

Furthermore, amended independent **claim 22** recites (among other limitations):

> a **general-purpose means for executing** a target process;
> a ROM-embedded means **for interrupting the execution of the target process** ..., the interrupting means being **executable by the target process executing means**;
> a ROM-embedded means for disassembling ..., the disassembling means being **executable by the target process executing means**;
> ...
> a ROM-embedded means for capturing a trace ..., the trace capturing means being **executable by the target process executing means**.

Also, amended independent **claim 24** recites (among other limitations):

> **a general-purpose processor**;
> ...
> a target process having executable instructions that are **executable by the general-purpose processor**; and
> a debugger program embedded within the ROM and having a disassembler and a trace capturer that are **executable by the general-purpose processor**;
> and wherein:
> the debugger program **interrupts execution of the target process** at some of the instructions; ....

In addition, amended independent **claim 29** recites (among other limitations):

> **a general-purpose processor**;
> a target process having executable instructions that are **executable by the general-purpose processor**; and
> a debugger program that is **executable by the general-**

purpose processor;

and wherein:

when the switch is off, the debugger program cannot be **launched in the general-purpose processor**; and

when the switch is on, the debugger program can be **launched in the general-purpose processor** to **interrupt execution of the target process** in the **general-purpose** processor at some of the instructions and operate on at least some of the instructions at which the execution of the target process is interrupted.

Further, amended independent **claim 30** recites (among other limitations):

launching, in a **general-purpose processor** of the computer system, a debugger program from a read-only memory (ROM) of the computer system, the ROM having a boot process and the debugger program embedded therein, the debugger program having a disassembler and a trace capturer;

interrupting execution, in the general-purpose processor, **of the target process** at an instruction; ....

Additionally, amended independent **claim 33** recites (among other limitations):

when the switch is set to the off state, preventing **execution of a debugger program in a general-purpose processor** of the computer system; and

when the switch is set to the on state:

launching the debugger program in the general-purpose processor;

interrupting, in the general-purpose processor, **execution of the target process** at an instruction; and

the debugger program **operating, in the general-purpose processor**, on the instruction.

Applicant respectfully submits that *Corti, et al.* does not teach or suggest these limitations. (Amendments to independent **claims 1, 11, 19, 22, 24, 29, 30 and 33** are supported in the specification at [0018].

Corti, et al. appears to disclose a **real-time** system-on-chip (SOC) with **signal processing logic** (i.e., **DSP** core) and an on-chip logic analysis (OCLA) unit . The OCLA unit includes a VHDL macro 14 that monitors the signal processing logic. The VHDL macro 14 is a **hardware component** embedded in the chip. The VHDL macro 14 is **completely separate physically** from the signal processing logic in the chip. By being **separate** from, but integrated on the same chip as, the monitored

component (the signal processing logic), the VHDL macro 14 can provide real-time data acquisition **without interrupting operations** of the monitored component. (See Figs. 1 and 2; column 1, lines 53-67; and column 2, lines 15-48.) The technique in *Corti, et al.* **expressly must not interrupt** operations of the monitored component, due to the **real-time** nature of the operation of the signal processing logic, wherein "stopping the processor could drive an invalid control signal to the actuator, which may cause a disastrous result." (Column 1, lines 26-39.) *Corti, et al.* is, therefore, **expressly different** from the claimed subject matter, which calls for execution of **both** the target process and the debugger program by the same general-purpose processor (instead of a specific-purpose real-time processor), wherein execution of the instructions of the target process is **interrupted** in order for the debugger program to operate on the instructions. Therefore, the real-time nature of the signal processing logic (the DSP core) in *Corti, et al.* means that the SOC cannot be considered to be the equivalent of the claimed general-purpose processor, since the signal processing logic **expressly cannot be interrupted**. Thus, the system in *Corti, et al.* apparently does not teach or fairly suggest a process and a debugger program (embedded in a ROM and **interrupting** and operating on instructions of the process), both of which run on the **same general-purpose processor** (or executing means), as called for in the amended independent **claims 1, 11, 19, 22, 24, 29, 30 and 33**. As a result, *Corti, et al.* also apparently does not teach or fairly suggest a disassembler and a trace capturer (or a disassembling means or trace means) that are **executable by the processor** (or the executing means), called for in amended independent **claims 22, 24 and 30**. Applicant respectfully submits, therefore, that independent **claims 1, 11, 19, 22, 24, 29, 30 and 33**, as amended, are not anticipated by, are not obvious in view of, and are patentable over *Corti, et al.* at least because the reference does not teach or fairly suggest these limitations.

Regarding dependent claims: Since **claims 2-5, 7-10, 12, 13, 15-18, 20-26, 28, 31 and 32** depend from amended independent claims **1, 11, 19, 22, 24 and 30**, Applicant respectfully submits that these claims also are not anticipated by, are not

obvious in view of, and are patentable over *Corti, et al.* at least for the same reasons.

Rejection Under 35 USC 103(a):

Applicant respectfully traverses the rejection of **claims 6, 14 and 27** under 35 U.S.C. 103(a) as being unpatentable over *Corti, et al.*, in view of *Case, et al.* **Claims 6, 14 and 27** depend from amended independent claims 1, 11 and 24, which are not anticipated by, are not obvious in view of, and are patentable over *Corti, et al.*, as described above. Applicant submits that *Case, et al.* does not cure the above-described deficiencies of *Corti, et al.* Therefore, Applicant respectfully submits that dependent **claims 6, 14 and 27**, as well as the rest of the claims, are not anticipated by, are not obvious in view of, and are patentable over *Corti, et al.*, in view of *Case, et al.* at least because the references do not teach or fairly suggest a process and a debugger program which run on the **same general-purpose processor**, such that the debugger program **interrupts** and operates on instructions of the process.

Conclusion:

For the reasons specifically discussed above, and others, it is believed that pending **claims 1-33** define patentable subject matter. Reconsideration of the previous rejections and objections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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